NEC

MOS INTEGRATED CIRCUIT

μPD23C4001EJ

4M-BIT MASK-PROGRAMMABLE ROM
512K-WORD BY 8-BIT

Description

The μPD23C4001EJ is a 4,194,304 bits (524,288 words by 8 bits) mask-programmable ROM.

The active levels of OE (Output Enable Input) can be selected with mask-option.

The μPD23C4001EJ is packed in 32-pin plastic DIP, 32-pin plastic SOP and 40-pin plastic TSOP (I).

Features

- Word organization : 524,288 words by 8 bits
- Wide voltage range: V_{CC} = 2.7 V to 5.5 V

Operating supply voltage V_{CC}	Access time ns (MAX.)	Operating ambient temperature °C	Power supply current (Active mode) mA (MAX.)	Standby current (CMOS level input) μA (MAX.)
5.0 V ± 10 %	120	–10 to +70	35	100
3.3 V ± 0.3 V	300	–10 to +70	15	25
	330	–20 to +85	20	150
3.0 V ± 0.3 V	350	–10 to +70	10	20
	380	–20 to +85	15	100

Ordering Information

Part Number	Package
μPD23C4001EJCZ-×××	32-pin Plastic DIP (600 mil)
μPD23C4001EJGW-×××	32-pin Plastic SOP (525 mil)
μPD23C4001EJGZ-×××-LJH	40-pin Plastic TSOP (I) (10 × 20 mm) (Normal bent)
μPD23C4001EJGZ-×××-LKH	40-pin Plastic TSOP (I) (10 × 20 mm) (Reverse bent)

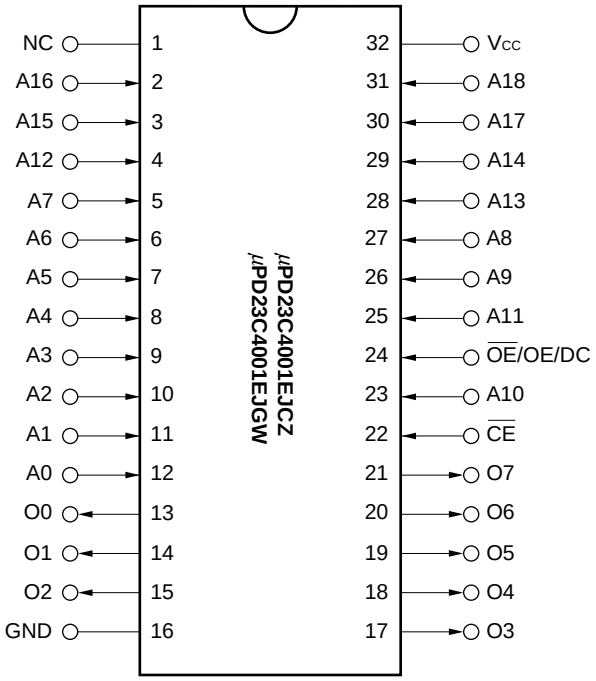
(×××: ROM code suffix No.)

The information in this document is subject to change without notice.

Document No. M10759EJ2V1DS00 (2nd edition)
Date Published May 1997 N
Printed in Japan

Pin Configuration (Marking Side)

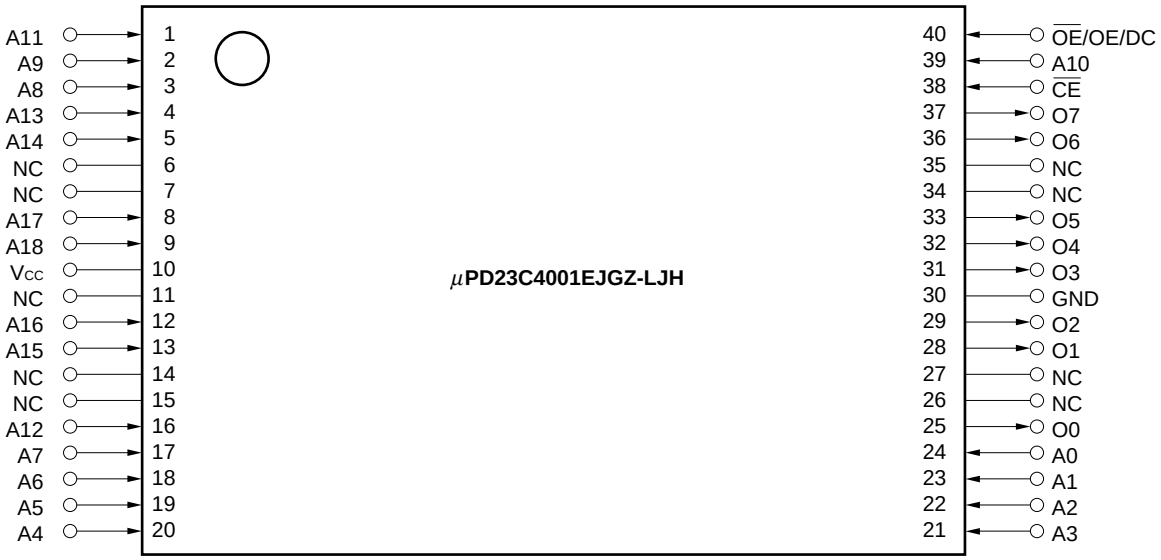
32-pin Plastic DIP (600 mil)
32-pin Plastic SOP (525 mil)



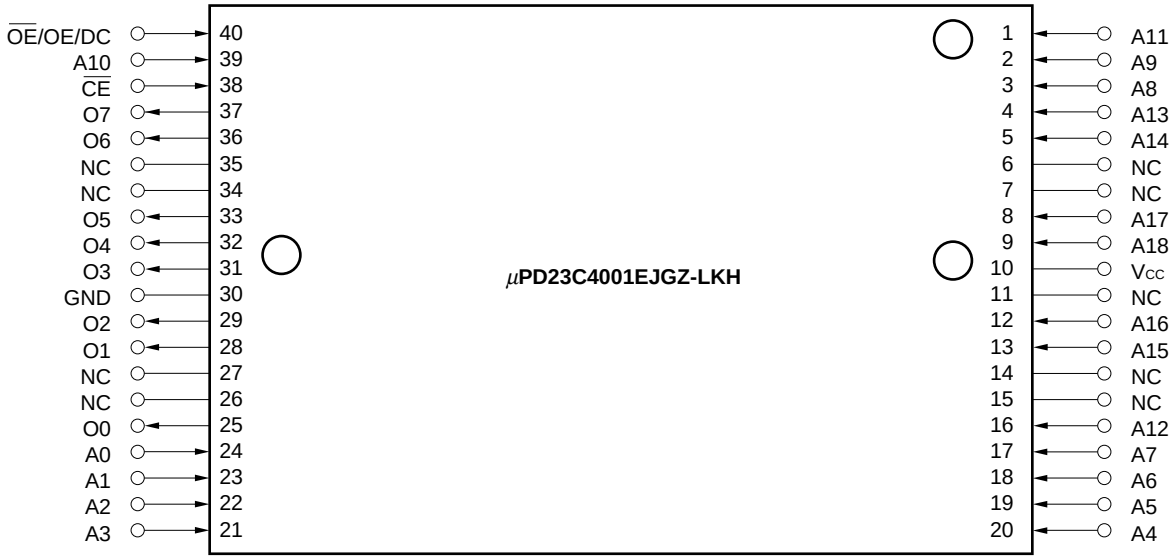
A0 - A18 : Address inputs
O0 - O7 : Data outputs
$\overline{CE}$: Chip enable
$\overline{OE}$/OE : Output enable
V_{CC} : Supply voltage
GND : Ground
NC[Note] : No connection
DC : Don't care

Note Some signals can be applied because this pin is not connected to the inside of the chip.

40-pin Plastic TSOP (I) (10 × 20 mm) (Normal bent)



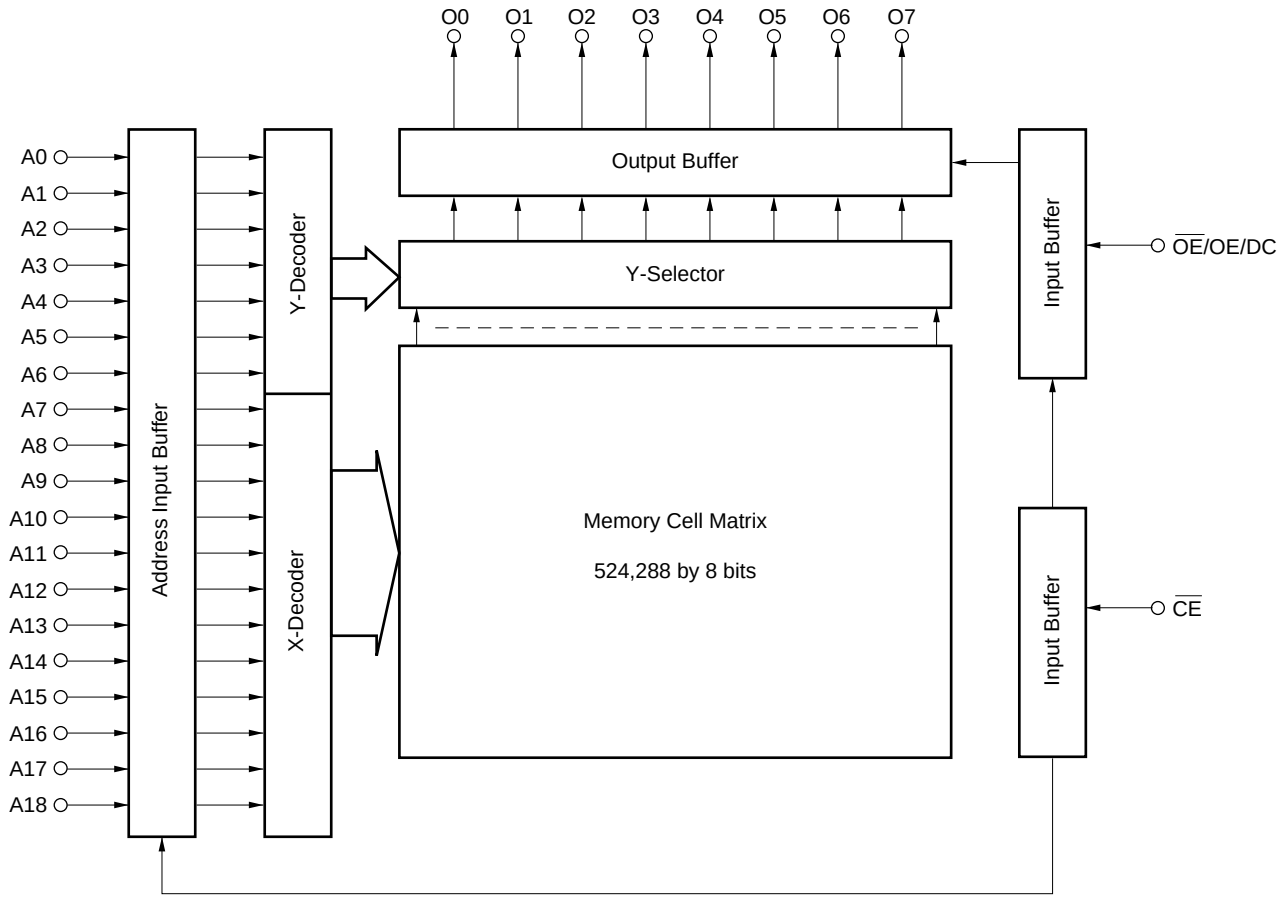
40-pin Plastic TSOP (I) (10 × 20 mm) (Reverse bent)



Input/Output Pin Functions

Pin name	Input/Output	Function
A0 to A18 (Address inputs)	Input	Address bus.
O0 to O7 (Data outputs)	Output	Output data bus.
$\overline{CE}$ (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are followings. High level ·····High impedance Low level ·····Data out
$\overline{OE}$/OE/DC (Output Enable/Don't care)		Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V_{CC}	—	Supply voltage
GND	—	Ground
NC	—	Not internally connected. (The signal can be connected.)

Block Diagram



Mask Option

The active levels of output enable pin ($\overline{OE}$/OE/DC) are mask programmable and optional, and can be selected from among “0” “1” “×” shown in the table below.

Option	$\overline{OE}$/OE/DC	OE active level
0	$\overline{OE}$	L
1	OE	H
×	DC	Don’t care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

$\overline{CE}$	$\overline{OE}$	Mode	Output state
L	L	Active	Data out
	H		High impedance
H	H or L	Standby	High impedance

Operation mode (Option : 1)

$\overline{CE}$	OE	Mode	Output state
L	L	Active	High impedance
	H		Data out
H	H or L	Standby	High impedance

Operation mode (Option : ×)

$\overline{CE}$	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High impedance

Remark L: Low level input
H: High level input

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		–0.3 to +7.0	V
Input voltage	V_I		–0.3 to V_{CC} +0.3	V
Output voltage	V_O		–0.3 to V_{CC} +0.3	V
Operating ambient temperature	T_A	V_{CC} = 5.0 V ± 10 %	–10 to +70	˚C
		V_{CC} = 2.7 V to 3.6 V	–20 to +85	
Storage temperature	T_{stg}		–65 to +150	˚C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance (T_A = +25 ˚C)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			15	pF
Output capacitance	C_O				15	pF

DC Characteristics 1 (T_A = –10 to +70 °C, V_{CC} = +5.0 V ± 10 %)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		2.2		V_{CC}+0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
High level output voltage	V_{OH1}	I_{OH} = –400 μA	2.4			V
	V_{OH2}	I_{OH} = –100 μA	V_{CC} –0.5			
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Input leakage current	I_{LI}	V_I = 0 to V_{CC}	–10		+10	μA
Output leakage current	I_{LO}	V_O = 0 to V_{CC}, Chip deselected	–10		+10	μA
Power supply current	I_{CC1}	$\overline{CE}$ = V_{IL} (Active mode), I_O = 0 mA			35	mA
Standby current	I_{CC2}	$\overline{CE}$ = V_{IH} (Standby mode)			1.5	mA
	I_{CC3}	$\overline{CE}$ = V_{CC}–0.2 V (Standby mode)			100	μA

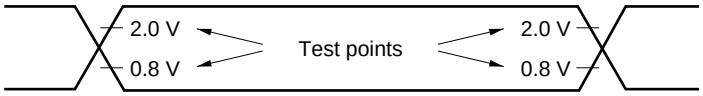
AC Characteristics 1 (T_A = –10 to +70 °C, V_{CC} = +5.0 V ± 10 %)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Address access time	t_{ACC}				120	ns
Chip enable access time	t_{CE}				120	ns
Output enable access time	t_{OE}				60	ns
Output hold time	t_{OH}		0			ns
Output disable time	t_{DF}		0		30	ns

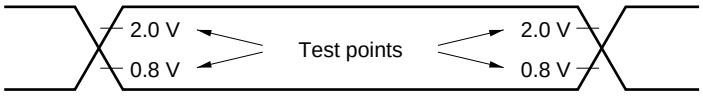
Remark t_{DF} is the time from inactivation of $\overline{CE}$ or $\overline{OE}$/OE to high-impedance state output.

AC Test Conditions

Input waveform (Rise/Fall time ≤ 5 ns)



Output waveform



Output load

1TTL + 100 pF

DC Characteristics 2 (T_A = –10 to +70 °C, V_{CC} = 2.7 V to 3.6 V)

Parameter	Symbol	Test conditions		MIN.	MAX.	Unit
High level input voltage	V_{IH}			0.7V_{CC}	V_{CC}+0.3	V
Low level input voltage	V_{IL}			–0.3	0.2V_{CC}	V
High level output voltage	V_{OH}	I_{OH} = –100 μA		0.8V_{CC}		V
Low level output voltage	V_{OL}	I_{OL} = 1.0 mA			0.4	V
High level input leakage current	I_{LIH}	V_I = V_{CC}			10	μA
Low level input leakage current	I_{LIL}	V_I = 0 V			–10	μA
High level output leakage current	I_{LOH}	V_O = V_{CC} Chip deselected			10	μA
Low level output leakage current	I_{LOL}	V_O = 0 V Chip deselected			–10	μA
Power supply current	I_{CC1}	$\overline{CE}$ = V_{IL} (Active mode), I_O = 0 mA	V_{CC} = 3.3 ± 0.3 V		15	mA
			V_{CC} = 3.0 ± 0.3 V		10	
Standby current	I_{CC3}	$\overline{CE}$ = V_{CC}–0.2 V (Standby mode)	V_{CC} = 3.3 ± 0.3 V		25	μA
			V_{CC} = 3.0 ± 0.3 V		20	

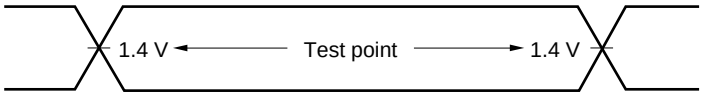
AC Characteristics 2 (T_A = –10 to +70 °C, V_{CC} = 2.7 V to 3.6 V)

Parameter	Symbol	V_{CC} = 3.0 ± 0.3 V		V_{CC} = 3.3 ± 0.3 V		Unit
		MIN.	MAX.	MIN.	MAX.	
Address access time	t_{ACC}		350		300	ns
Chip enable access time	t_{CE}		350		300	ns
Output enable access time	t_{OE}		150		120	ns
Output hold time	t_{OH}	0		0		ns
Output disable time	t_{DF}	0	50	0	40	ns

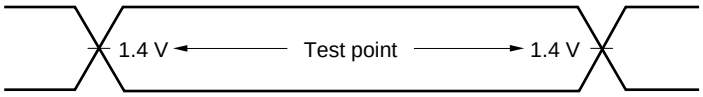
Remark t_{DF} is the time from inactivation of $\overline{CE}$ or $\overline{OE}$/OE to high-impedance state output.

AC Test Conditions

Input waveform (Rise/Fall time ≤ 5 ns)



Output waveform



Output load

1TTL + 100 pF

DC Characteristics 3 (T_A = –20 to +85 °C, V_{CC} = 2.7 V to 3.6 V)

Parameter	Symbol	Test conditions		MIN.	MAX.	Unit
High level input voltage	V_{IH}			0.7V_{CC}	V_{CC}+0.3	V
Low level input voltage	V_{IL}			–0.3	0.17V_{CC}	V
High level output voltage	V_{OH}	I_{OH} = –100 μA		0.8V_{CC}		V
Low level output voltage	V_{OL}	I_{OL} = 1.0 mA			0.5	V
High level input leakage current	I_{LIH}	V_I = V_{CC}			20	μA
Low level input leakage current	I_{LIL}	V_I = 0 V			–20	μA
High level output leakage current	I_{LOH}	V_O = V_{CC} Chip deselected			20	μA
Low level output leakage current	I_{LOL}	V_O = 0 V Chip deselected			–20	μA
Power supply current	I_{CC1}	$\overline{CE}$ = V_{IL} (Active mode), I_O = 0 mA	V_{CC} = 3.3 ± 0.3 V		20	mA
			V_{CC} = 3.0 ± 0.3 V		15	
Standby current	I_{CC3}	$\overline{CE}$ = V_{CC}–0.2 V (Standby mode)	V_{CC} = 3.3 ± 0.3 V		150	μA
			V_{CC} = 3.0 ± 0.3 V		100	

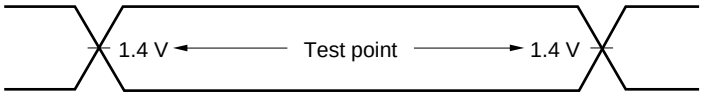
AC Characteristics 3 (T_A = –20 to +85 °C, V_{CC} = 2.7 V to 3.6 V)

Parameter	Symbol	V_{CC} = 3.0 ± 0.3 V		V_{CC} = 3.3 ± 0.3 V		Unit
		MIN.	MAX.	MIN.	MAX.	
Address access time	t_{ACC}		380		330	ns
Chip enable access time	t_{CE}		380		330	ns
Output enable access time	t_{OE}		170		140	ns
Output hold time	t_{OH}	0		0		ns
Output disable time	t_{DF}	0	50	0	40	ns

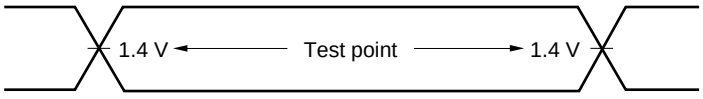
Remark t_{DF} is the time from inactivation of $\overline{CE}$ or $\overline{OE}$/OE to high-impedance state output.

AC Test Conditions

Input waveform (Rise/Fall time ≤ 5 ns)



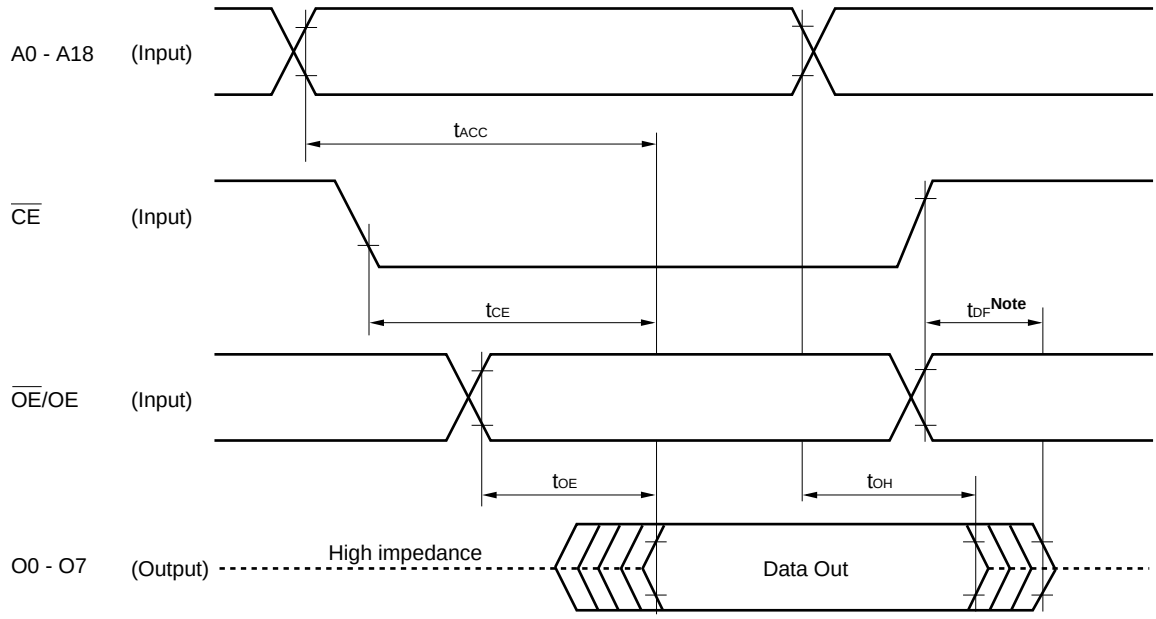
Output waveform



Output load

1TTL + 100 pF

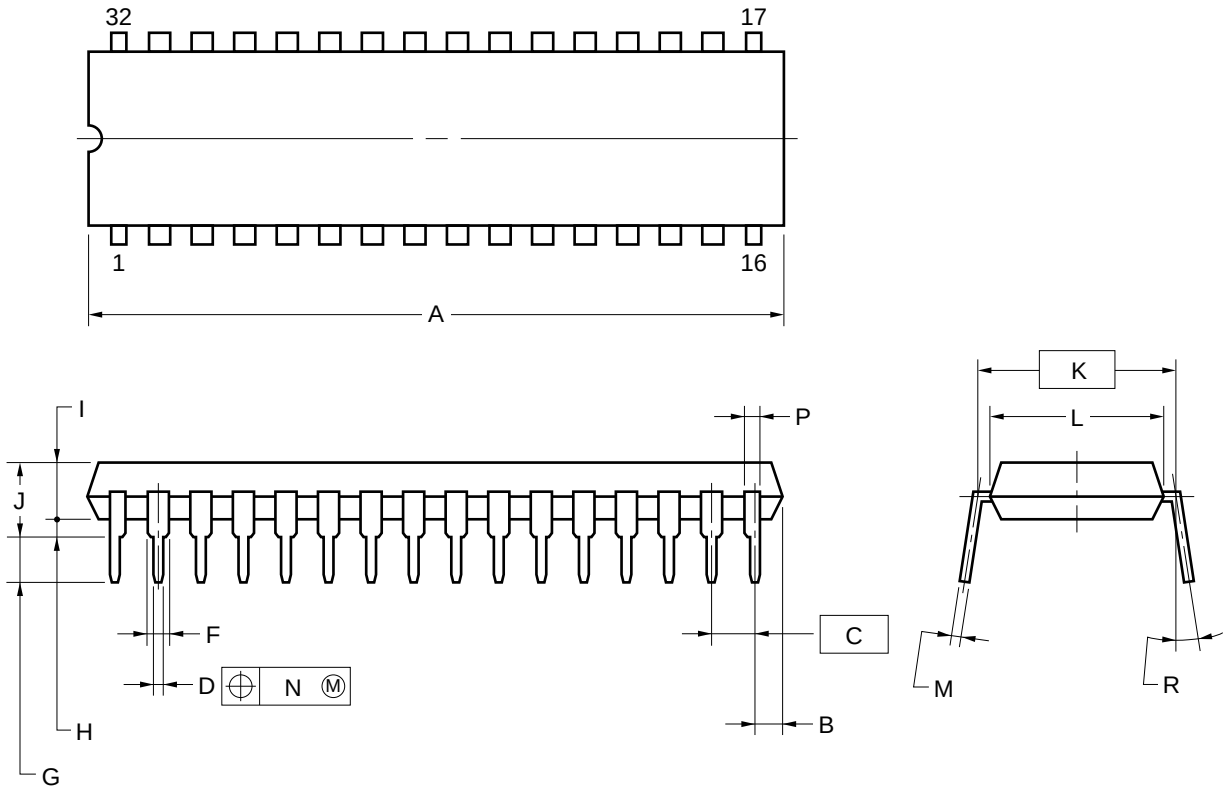
Read Cycle Timing Chart



Note t_{DF} is specified when the one of $\overline{CE}$, $\overline{OE}$/OE is inactivated.

Package Drawings

32PIN PLASTIC DIP (600 mil)



NOTES

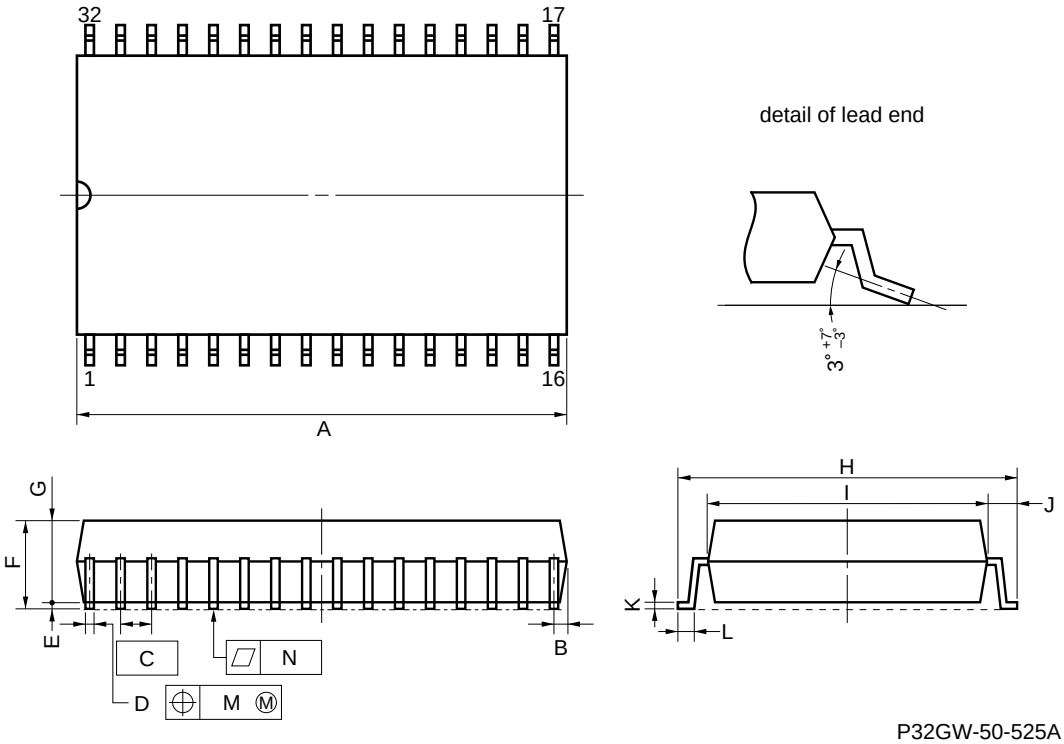
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	40.64 MAX.	1.600 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.
R	0~15°	0~15°

P32C-100-600A-1

32 PIN PLASTIC SOP (525 mil)



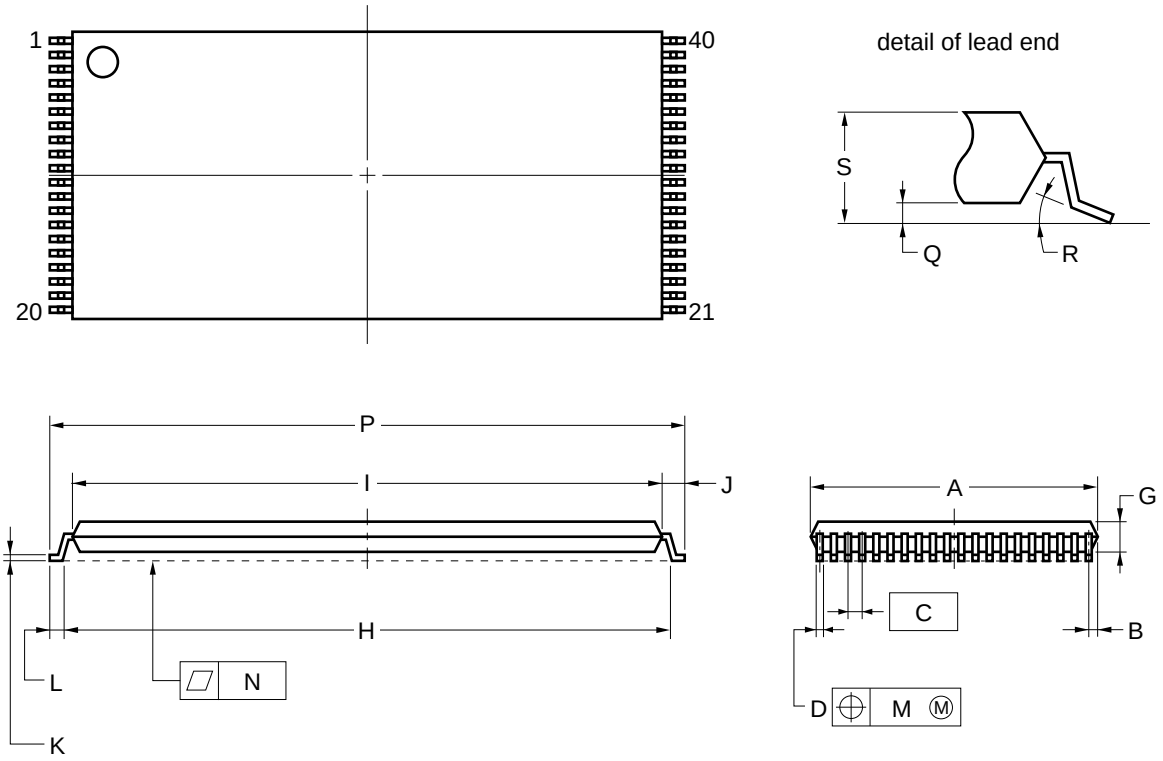
P32GW-50-525A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.61 MAX.	0.812 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.15±0.05	0.006
F	2.95 MAX.	0.117 MAX.
G	2.7	0.106
H	14.1±0.3	0.555±0.012
I	11.3	0.445
J	1.4±0.2	0.055±0.008
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004

40 PIN PLASTIC TSOP (I) (10×20)



NOTES

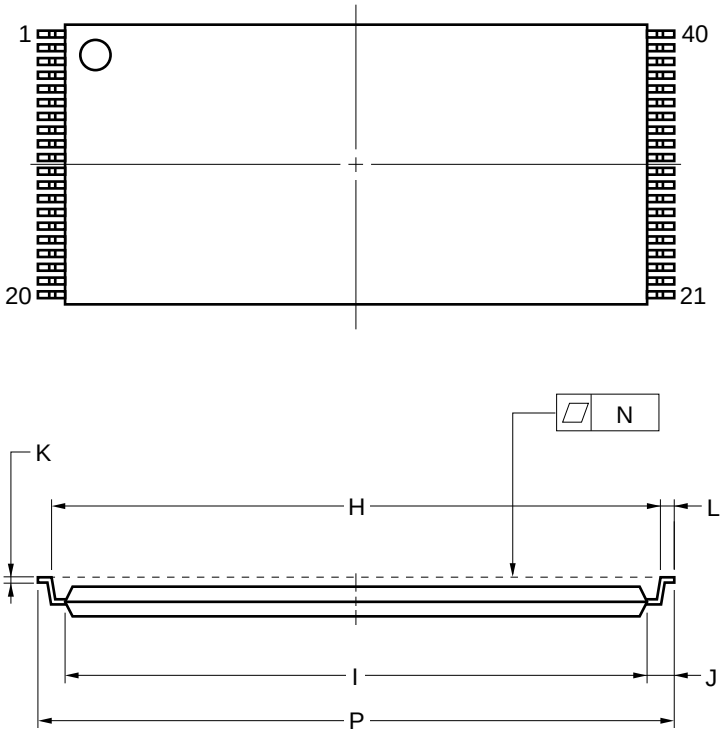
(1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

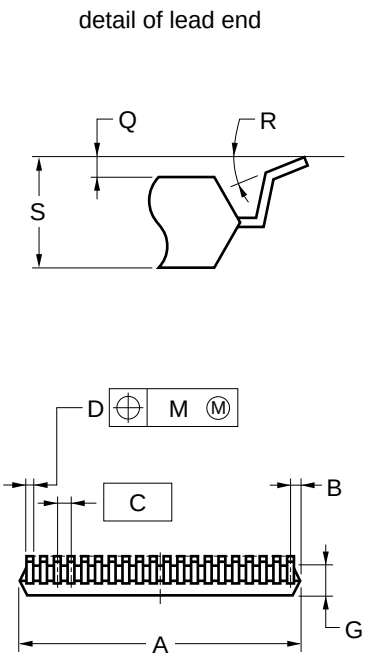
(2) "A" excludes mold flash. (Includes mold flash : 10.4 mm MAX. <0.410 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	10.0±0.1	$0.394^{+0.004}_{-0.005}$
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.20±0.10	0.008±0.004
G	1.02 MAX.	0.041 MAX.
H	19.0±0.2	0.748±0.008
I	18.4±0.2	$0.724^{+0.009}_{-0.008}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.08	0.003
N	0.10	0.004
P	20.0±0.2	$0.787^{+0.009}_{-0.008}$
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.1 MAX.	0.044 MAX.

S40GZ-50-LJH-2

40 PIN PLASTIC TSOP (I) (10×20)





NOTES

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(2) "A" excludes mold flash. (Includes mold flash : 10.4 mm MAX. <0.410 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	10.0±0.1	$0.394^{+0.004}_{-0.005}$
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.20±0.10	0.008±0.004
G	1.02 MAX.	0.041 MAX.
H	19.0±0.2	0.748±0.008
I	18.4±0.2	$0.724^{+0.009}_{-0.008}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.08	0.003
N	0.10	0.004
P	20.0±0.2	$0.787^{+0.009}_{-0.008}$
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.1 MAX.	0.044 MAX.

S40GZ-50-LKH-2

Recommended Soldering Conditions

The following conditions (see table below) must be met when soldering the μPD23C4001EJ.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

Please consult our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Types of Surface Mount Device

μPD23C4001EJGW : 32-pin Plastic SOP (525 mil)

μPD23C4001EJGZ-LJH : 40-pin Plastic TSOP (I) (10 × 20 mm) (Normal bent)

μPD23C4001EJGZ-LKH : 40-pin Plastic TSOP (I) (10 × 20 mm) (Reverse bent)

Please consult with our sales offices.

Type of Through Hole Mount Device

μPD23C4001EJCZ : 32-pin Plastic DIP (600 mil)

Soldering process	Soldering conditions
Wave soldering (Only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Partial heating method	Terminal temperature: 300 °C or below, Time: 3 seconds or below (Per one lead)

Caution Do not jet molten solder on the surface of package.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by the customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

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